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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID ALAN EWARD, MARGARET ROSE GEARTY,
GLENN A. FARRALL, ATSUSHI HASEGAWA,
and ANTHONY WILLIS RICH

Appeal 2009-003922
Application 09/411,792
Technology Center 2100

Decided: February 23, 2010

Before JOSEPH L. DIXON, JEAN R. HOMERE, and JAY P. LUCAS,
Administrative Patent Judges.

DIXON, *Administrative Patent Judge.*

DECISION ON APPEAL

The Appellants appeal under 35 U.S.C. § 134(a) from a Final
Rejection of claims 1-64. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

I. STATEMENT OF THE CASE

The Invention

Appellants' invention relates to a method and an interface for debugging processors and transferring debug information (Spec. 1).

The Illustrative Claim

Claim 1, an illustrative claim, reads as follows:

1. A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

The References

The Examiner relies on the following references as evidence:

Circello	U.S. 5,737,516	Apr. 7, 1998
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William Hohl, Joe Circello, and Klaus Riedel, *Debug Support on the ColdFire Architecture*, Motorola, Inc. Austin TX, pages. 1-10 (May 1996) (hereinafter "Hohl").

The Rejections

The following rejections are before us for review:

Claims 1-64 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hohl and Circello.

II. ISSUES

Have the Appellants shown that the Examiner erred in using two references for the anticipation rejection of the claimed limitations?

Have the Appellants shown that the Examiner erred in finding that Hohl discloses “the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored,” as recited in claim 1?

III. PRINCIPLES OF LAW

Prima Facie Case of Unpatentability

Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner’s position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Anticipation

“[A]nticipation of a claim under § 102 can be found only if the prior

art reference discloses every element of the claim” *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1457 (Fed. Cir. 1984)). “[A]bsence from the reference of any claimed element negates anticipation.” *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986). In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

IV. FINDINGS OF FACT

The following findings of fact (FFs) are supported by a preponderance of the evidence.

Hohl

1. The Hohl reference has three authors; William Hohl, Joe Circello, and Klaus Riedel. The Circello reference only has two inventors; Joe Circello and William Hohl.

2. Hohl discloses a sample code in Fig. 7 for PST/DDATA synchronization (Hohl, fig. 7, page 6). Hohl also discloses that PST/DDATA signal is the output signal of the Debug module in Fig. 3 (fig. 3, page 2).

3. Hohl further discloses that a K-Bus, a high-speed, single cycle bus, connects the processor core, internal memories, and the debug module for transmitting data (fig. 3, page 2).

V. ANALYSIS

The Examiner set forth in detail a prima facie case of unpatentability in the Examiner's Answer. Therefore, we look to Appellants' Briefs to show error in the proffered prima facie case.

The Common Feature in Claims

Independent claim 1, recites, *inter alia*, "the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored." Independent claims 21 and 42 contain similar limitations.

35 U.S.C. § 102(b) rejections

With respect to independent claim 1, Appellants contend that the Examiner's § 102(b) rejection is improper because "it appears the Examiner has attempted to reject the claims based on some combination of Circello and MotorlaNPL, but has failed to establish what the system resulting from the combination of these two references would [look] like or why one of the skill in the art would have combined these two references." (App. Br. 11).

The Examiner states that Hohl and Circello "clearly discuss the same debug module. . . . It would be unnecessary for obviousness under 35 USC 103(a)." (Ans. 15).

We disagree with the Examiner's statement. We find that the two references have different inventors/authors (inventive entities), and that they are different prior art references (FF 1). The *Manual of Patent Examining Procedure* (MPEP) states:

Normally, only one reference should be used in making a rejection under 35 U.S.C. 102. However, a 35 U.S.C. 102 rejection over multiple references has been held to be proper when the extra references are cited to:

- (A) Prove the primary reference contains an "enabled disclosure;"
- (B) Explain the meaning of a term used in the primary reference; or
- (C) Show that a characteristic not disclosed in the reference is inherent.

(MPEP § 2131.01).

We also find that the Examiner uses either the Hohl or the Circello reference beyond the above mentioned three limited circumstances permitted under MPEP § 2131.01, and thus under 35 U.S.C. § 102(b). "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. USA v Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991). Here, in both the Final Rejection filed on Jan. 10, 2008 and the

statement of the rejection presented in the Examiner's Answer, the Examiner used the combination of the teachings of Hohl and Circello to reject the claimed limitations (*e. g.*, Final Rejection 4; Ans. 4 and 6). Therefore, we agree with the Appellants that the anticipation rejection under 35 U.S.C. § 102 was improper.

The Appellants further contend that neither of the cited references discloses transmitting an operand address from a processor to a debug circuit because when the instruction at the address 00001318 in Fig. 7 is executed "the DDATA signal transmits the operand values for this instruction" (Reply Br. 2), "[a]s such, the Examiner's contention that the instruction address '0001318' is in the KADDR signal on the K-bus at the same that the operand values for the instruction stored at this address are on the DDATA bus is entirely unsupported." (Reply Br. 3).

We agree with the Appellants' contentions. We find that Hohl teaches that the DDATA signal is the output signal of the debug module (FF 2), which is not the signal transmitted from the processor to the debug module. The KADDR signal on the K-Bus is transmitted from the processor to the debug module and is not related to the instruction address 00001318 or the Fig. 7 cited by the Examiner (FF 3). Thus, we conclude that one skilled in the art could not make the inherency reasoning that the instruction address 00001318 at the DDATA signal is the operand address in the KADDR signal on the K-Bus as maintained by the Examiner.

Because we agree with at least one of the Appellants' contentions, we find that the Examiner has not made a requisite showing of anticipation as

required to disclose the invention as recited in claim 1 by Hohl. The rejection of dependent claims 2-20 and 61 contains the same deficiency. Appellants, thus, have demonstrated error in the Examiner's conclusion of anticipation for the subject matter of claims 1-20 and 61.

The independent claims 21 and 42 contain similar limitations to those found in independent claim 1. Appellants present similar arguments as set forth with respect to independent claim 1 in response to the rejections of independent claims 21 and 42 (App. Br. 7 and 10; Reply Br. 1-2).

As we found above in our discussion with respect to independent claim 1, we find that Appellants have demonstrated error in the Examiner's conclusion of anticipation for the subject matter of independent claims 21, 22, and 42. The rejection of dependent claims 23-41, 43-60, and 62-64 contains the same deficiency. Hence, Appellants' argument persuades us that the Examiner erred in rejecting claims 1-64.

We, therefore, cannot sustain the rejection of claims 1-64 under 35 U.S.C. § 102 (b).

VI. CONCLUSION

We conclude that the Appellants have shown that the Examiner erred in using two references for the anticipation rejection under 35 U.S.C. § 102(b) of the claimed limitations.

We conclude that the Appellants have shown that the Examiner erred in identifying that Hohl discloses "the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values

Appeal 2009-003922
Application 09/411,792

each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored,” as recited in claim 1 and similarly in independent claims 21, 22, and 42.

VII. DECISION

We reverse the anticipation rejection of claims 1-64 under 35 U.S.C. § 102(b).

REVERSED

msc

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